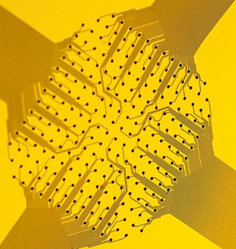
**Averatek’s A-SAP™ Process: Very High-Density Interconnect, Be Part of the Community**

2021 is a VERY exciting time for Averatek’s A-SAP™ process. There are currently three U.S. based fabricators licensing this technology and building panels, opening commercial capacity that has not previously been available in the US.

**Ability to Form 15-micron traces and spaces is proven**

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At this point, the ability to form a 15-micron trace and space with the A-SAP™ process has been well proven. While gathering reliability data is something that will not ever be “complete”, Averatek is also publishing results of tests including IST coupon testing and signal integrity analysis across a variety of materials.

**Now, let’s build a Community of Interest to take advantage of those benefits**

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The next step that Averatek is excited to announce is the launch of the **“A-SAP™ Community of Interest” content platform.** With commercial availability and proven reliability parameters, it is now time to build a community of experts from across all sectors of the electronics industry that understand this technology from a fabrication perspective and understand how to apply this technology to **optimize the benefits of 15-micron trace and space in PCB design**. As with any technology advancement, this capability will have impacts across the full supply chain: materials, design, fabrication, assembly, equipment, and standards.

This exciting semi- additive PCB fabrication process enables high-density PCB design opportunities coupled with **RF and signal integrity benefits** that were previously unavailable and provides a tremendous benefit to PCB designers. The installation of A-SAP™ is a relatively simple process that allows fabricators to meet the ever-intensifying HDI needs of their customers.

**Video from Industry Experts**

The short video, link below, announcing the A-SAP™ Community of Interest platform, lets us hear from several designers and fabricators, in their own words, express why they are excited for this technology breakthrough and **why they believe this is important for the industry**.

**Kelly Dack** comments that the design world will need to be prepared to have their small scall design challenges rocked. **Cherie Litson** is excited that Averatek’s A-SAP™ process eliminates pin out challenges while maintaining reliable signal integrity and **Randy Chase** clearly articulates the design requirements that are driving him to require line and spaces at 50 micron, something that is not reliably and repeatedly available in the U.S. today with subtractive etch processes.

[Calumet Electronics](https://www.calumetelectronics.com/) is the first commercial fabricator to offer this technology. **Dr. Meredith LaBeau** expressed her thoughts advocating that designers and manufactures have the opportunity to collaborate to **“drop the SWaP”** while increasing the reliability and robustness of the most essential component, the printed circuit board. **Brad Bourne**, CEO of [FTG](https://www.ftgcorp.com/) is excited to work with Averatek’s advanced PCB fabrication process to **support their Aerospace and Defense customers** for years to come. **Anaya Vardya**, CEO of [American Standard Circuits](https://www.asc-i.com/) sees value in two areas, fine line, sub 2 mil trace and space feature sizes and the **ability to form conductors with gold rather than copper** conductors, a benefit becoming increasing important to the medical industry.

Materials suppliers play an integral role the PCB fabrication and PCB design process and there are several new materials coming to market. Material compatibility with A-SAP™ from both peel strength and signal integrity characterization, is something that most everyone is interested in as they consider how to best apply A-SAP™ technology. Reaching out to **Chris Hunrath**, Vice President of Technology at [Insulectro](https://www.insulectro.com/), he expands on the benefits of using a taller yet narrowing traces for signal integrity advantages, an important factor in this technology breakthrough. **Paul Cooke,** Field Applications Engineer and Technical Sales for [AGC-Nelco](https://agc-nelco.com/), is now on the materials side of the supply chain, with deep roots in PCB fabrication. He shares his thoughts on the advantage from both an RF perspective, eliminating the etch comp requirements, and the opportunity to significantly reduce layer count, simplifying complex designs.



[Altium’s](https://www.altium.com/) Director of Community and Industry Engagement, **Judy Warner**, is excited for the benefits that Averatek’s A-SAP™ process opens up for PCB design engineers including increased density, lower costs and benefits to SWaP.

As [Averatek’s](http://www.averatekcorp.com/) Vice President of Marketing and Business Development, I invite you to listen to this short video, visit our website, and join our mailing list to quickly receive new information and updates. The A-SAP™ Community of Interest Platform will be expanding quickly with content and comments from all areas of the electronics supply chain. As always if you have any specific questions about this technology, please reach out to me at **tara@averatek.com**.

Averatek A-SAP™ Community of Interest Content Platform Kick-off video link:

<https://www.youtube.com/watch?v=o_FM5HiRE28>